

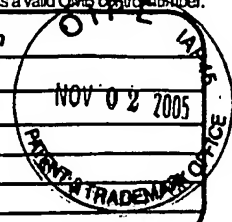
Substitute for form 1449A/PTO

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Sheet	1	of	2
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<b>Application Number</b>	10/003,951
<b>Filing Date</b>	October 30, 2001
<b>First Named Inventor</b>	Frederic Reblewski
<b>Art Unit</b>	2125
<b>Examiner Name</b>	A. Paladini
<b>Attorney Docket Number</b>	003921.00069

[illegible][illegible]

**Examiner  
Signature**

Altinpal.

**ALBERT W. PALADIN**  
**PATENT EXAMINER**

Date \_\_\_\_\_

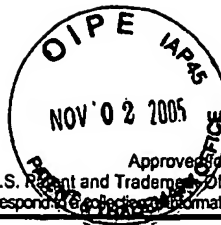
**Considered**

3-7-08

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PTO/SB/08b(08-03)

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Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 2 of 2

**Complete if Known**

Application Number	10/003,951
Filing Date	October 30, 2001
First Named Inventor	Frederic Reblewski
Art Unit	2125
Examiner Name	A. Paladini
Attorney Docket Number	003921.00069

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
Am		Y. NI, et al., "A 256 x 256 Pixel Smart CMOS Image Sensor for Line-Based Stereo Vision Applications", IEEE Journal of Solid-State Circuits, Vol. 35, No. 7, July 2000.	
Gm		Y. MIYAKE, et al., "A gesture controlled human interface using anartificial retina chip", IEEE, 1996.	
Ar		D.P. OSTERMAN, et al., "Superconducting Infrared Detector Arrays with Integrated Processing Circuitry", IEEE Transactions on Magnetics, Vol. 27, No. 2, March 1991.	
Am		H. AGUSLEO, et al., "Employing Logic-Enhanced Memory for High-Performance ATM Network Interfaces", IEEE, 1996.	
Am		R. de VRIES, et al., "Built-In Self-Test methodology for A/D Converters", IEEE, 1997.	
Ar		F. AZAIS, et al., "A Low-Cost Adaptive Ramp Generator for Analog BIST Applications", IEEE, 2001.	

Examiner Signature	 <b>ALBERT W. PALADINI</b> <b>PATENT EXAMINER</b>	Date Considered	3-7-06
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